VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Title:

Title has been amended to read as follows:

~~AN INTEGRATED DEVICE WITH A TRENCH~~ ISOLATION TRENCH STRUCTURE~~, AND FABRICATION PROCESS THEREFOR~~ FOR INTEGRATED DEVICES

In the Specification:

Paragraph beginning at line 1 of page 3 has been amended as follows:

The process sequence that leads to an integrated device IC being defined with junction isolation wells IS, starts with a semiconductor material ~~1a~~1 of the N^- type and comprises an initial step of forming a first epitaxial region ~~1b~~11 of the N^- type, followed by a masking, implanting, and P-dopant diffusing step to form a buried layer ~~1c~~12 of the isolation well.

Paragraph beginning at line 6 of page 3 has been amended as follows:

In particular, the buried layer ~~1c~~12, additionally to providing part of the buried insulator for the drive circuitry or region LV, provides here part of the base region of the NPN power component or region HV.

Paragraph beginning at line 9 of page 3 has been amended as follows:

A subsequent masking, implanting, and N-dopant diffusing step, carried out at the buried layer ~~1c~~12, will bulk delimit the N-type regions 2 intended to contain various circuitry components, as described in connection with the prior art shown in Figure 1.

Paragraph beginning at line 12 of page 3 has been amended as follows:

The buried layer ~~1c~~12, besides providing the emitter for the NPN power component in the region HV, also functions as a buried collector and buried drain for the NPN and VDMOS signal components, respectively, in the region LV.

Paragraph beginning at line 15 of page 3 has been amended as follows:

An additional epitaxial region 3 is necessary to provide N-type isolated wells IS. These wells are fully delimited with an additional masking, implanting, and P-type diffusing step to form the isolation regions 4 in the epitaxial region 3 and ensure electrical continuity to the buried region ~~1c~~12.

Paragraph beginning at line 1 of page 4 has been amended as follows:

Note should be taken that the above conventional isolation well structures IS closely resemble each other. The only differences to be seen are in the substrate, of the P type or the N type, and the integration of the region ~~1c~~12 with VIPower technology.

Paragraph beginning at line 8 of page 5 has been amended as follows:

The features and advantages of the integrated device with an isolation structure, according to this invention, will be apparent from the following description of embodiments thereof, given by way of non-limitative examples with reference to the accompanying drawings, wherein:

Figure 1 is a schematic cross-sectional view of an integrated device with a junction type of isolation structure, according to the prior art;

Figure 2 is a schematic cross-sectional view of an integrated device with a junction type of isolation structure, as formed with a conventional low-power technology;

Figure 3 is a schematic cross-sectional view of an integrated device with a junction type of isolation structure, as formed with a conventional VIPower technology;

Figure 4 is a schematic cross-sectional view of an integrated device with a trench type of isolation structure, according to the invention; ~~and~~

Figures 5 to 5e show successive process steps for fabricating the integrated device with a trench type of isolation structure, according to the invention;~~.~~

Figure 6 is a schematic cross-sectional view of another embodiment of an integrated device formed in accordance with the present invention;

Figure 7 is a schematic cross-sectional view of another embodiment of an integrated device formed in accordance with the present invention;

Figure 8 is a schematic cross-sectional view of another embodiment of an integrated device formed in accordance with the present invention;

Figure 9 is a schematic cross-sectional view of another embodiment of an integrated device formed in accordance with the present invention; and

Figure 10 is a schematic cross-sectional view of another embodiment of an integrated device formed in accordance with the present invention.

In the Claims:

Claim 18 has been canceled.

Claims 1, 4, and 17 have been amended as follows:

1. (Amended) An integrated device, comprising: a substrate wherein a buried layer and an epitaxial region have been formed, and an isolation structure adapted to define a plurality of isolation wells for integrating the components of the integrated device therein, said isolation structure comprises plural dielectrically insulated trenches, each trench having an open bottom and each trench filled with a conductive material to form a ~~plurality of~~ contact ~~regions to buried regions of the device, said buried regions including, in particular,~~ region that is in direct contact with one of the substrate and buried layer.

4. (Amended) The integrated device of claim 2 wherein ~~each isolation well comprises, located at each of its edges, a~~ the plurality of trenches are in contact with said buried layer and are located at each edge of each isolation well.

17. (Amended) An isolation trench structure, comprising:

a substrate having a buried layer and an epitaxial region formed therein;

a plurality of isolation wells formed in the substrate; and

a dielectrically insulated trench formed ~~in intervening areas~~ between each of the isolation wells and located at the edges of the isolation wells, each trench having an open bottom and each trench comprising a central contact region surrounded by insulating dielectric regions.

each central contact region formed of electrically conductive material that is in direct contact with the buried layer.

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